SONY

CXD3301R

10-bit, 36Msps CCD Signal Processor

Description

The CXD3301R processes (correlated double sampling, programmable gain amplifier) the signals output from a CCD image sensor and performs conversion from analog signals to digital signals.

Features

- CCD signal processing
  - — Correlated double sampling (CDS)
  - — Programmable gain amplifier (PGA)
    Gain range: –6 to +42dB
- 10-bit resolution
  No missing code guaranteed

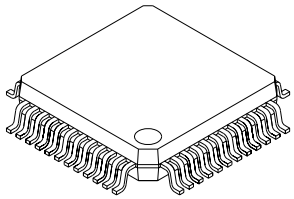
Applications

CCD cameras

Structure

Silicon gate CMOS IC

48 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	AV_{DD}, DV_{DD}	4.0	V
• Supply voltage difference (between AV_{DD} pins)		±0.1	V
• Ground voltage difference (between AV_{SS} pins)		±0.1	V
• Digital input voltage		–0.3 to +5.3	V
• Analog input voltage		–0.3 to AV_{DD} + 0.3	V
• Storage temperature	Tstg	–55 to +125	°C

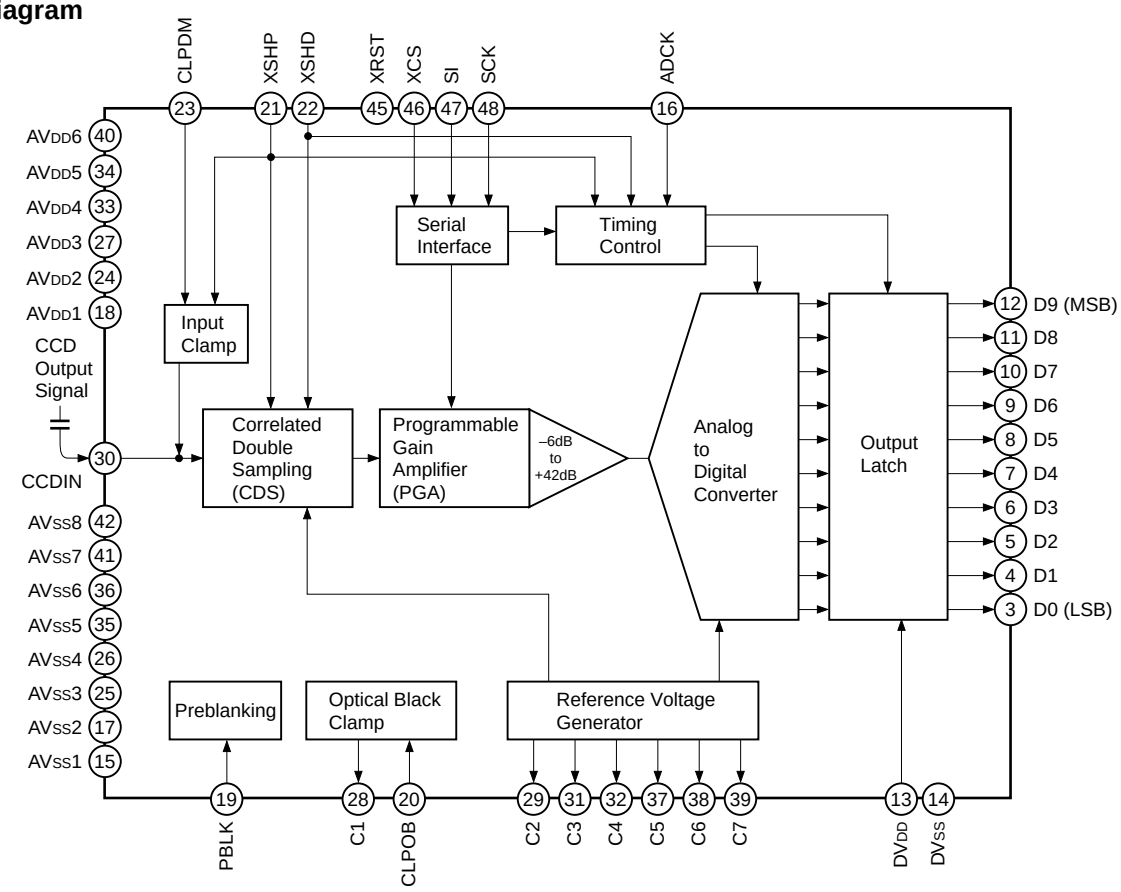
Note) If stress larger than the values listed under Absolute Maximum Ratings is applied, the device may be permanently damaged. Also note that applying the absolute maximum rating for long periods of time may affect the device reliability.

Recommended Operating Conditions

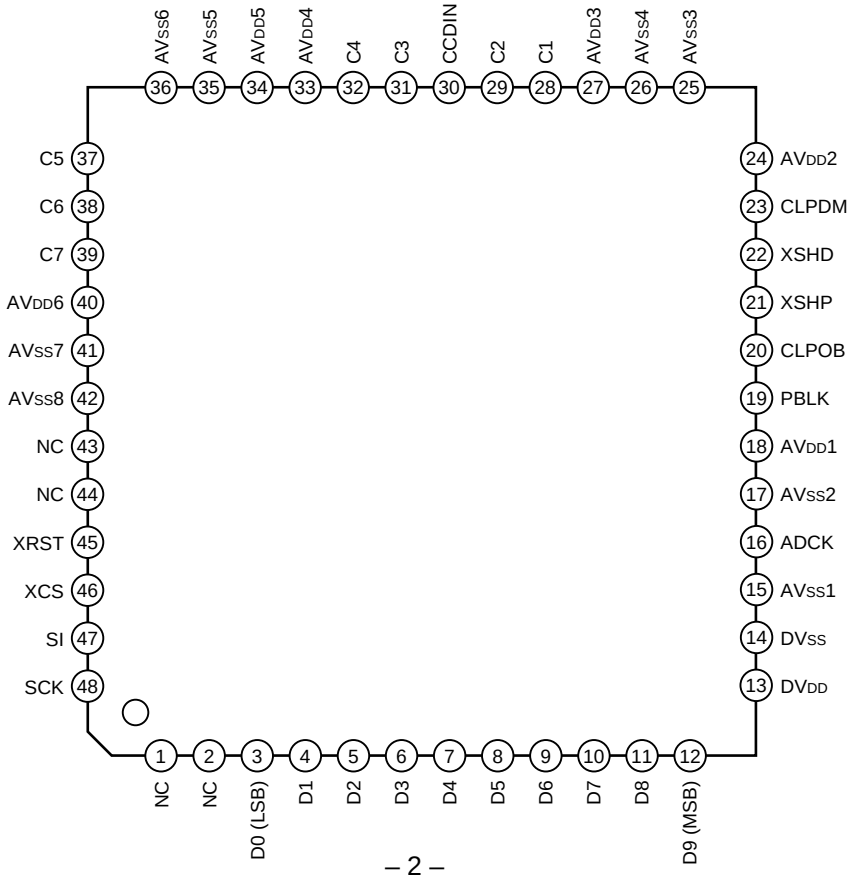
• Supply voltage	AV_{DD}, DV_{DD}	3.0 to 3.6	V
• Operating temperature	Topr	–20 to +75	°C

E01712

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	Type	Description
1	NC	—	(Always leave open.)
2	NC	—	(Always leave open.)
3	D0 (LSB)	DO	Bit 0, A/D output (LSB)
4	D1	DO	Bit 1, A/D output
5	D2	DO	Bit 2, A/D output
6	D3	DO	Bit 3, A/D output
7	D4	DO	Bit 4, A/D output
8	D5	DO	Bit 5, A/D output
9	D6	DO	Bit 6, A/D output
10	D7	DO	Bit 7, A/D output
11	D8	DO	Bit 8, A/D output
12	D9 (MSB)	DO	Bit 9, A/D output (MSB)
13	DV_{DD}	P	Power supply for digital output driver
14	DV_{SS}	P	GND for digital output driver
15	$AV_{SS}1$	P	Analog GND
16	ADCK	DI	Master clock
17	$AV_{SS}2$	P	Analog GND
18	$AV_{DD}1$	P	Analog power supply
19	PBLK	DI	Preblanking (High: Normal output, Low: All 0 output)
20	CLPOB	DI	Optical black clamp pulse
21	XSHP	DI	CCD signal precharge level sampling pulse
22	XSHD	DI	CCD signal data level sampling pulse
23	CLPDM	DI	Dummy bit clamp pulse
24	$AV_{DD}2$	P	Analog power supply
25	$AV_{SS}3$	P	Analog GND
26	$AV_{SS}4$	P	Analog GND
27	$AV_{DD}3$	P	Analog power supply
28	C1*2	AO	Optical black clamp circuit reference
29	C2*3	AO	Internal reference P
30	CCDIN	AI	CCD signal input
31	C3*4	AO	Internal reference C
32	C4*3	AO	Internal reference N
33	$AV_{DD}4$	P	Analog power supply
34	$AV_{DD}5$	P	Analog power supply
35	$AV_{SS}5$	P	Analog GND
36	$AV_{SS}6$	P	Analog GND

Pin No.	Symbol	Type	Description
37	C5*4	AO	A/D converter in-phase mode voltage
38	C6*4	AO	A/D converter high potential reference
39	C7*4	AO	A/D converter low potential reference
40	AVDD6	P	Analog power supply
41	AVSS7	P	Analog GND
42	AVSS8	P	Analog GND
43	NC	—	(Always leave open.)
44	NC	—	(Always leave open.)
45	XRST	DI	IC internal reset input (High: Normal operation, Low: Reset operation)
46	XCS	DI	Serial communication microcomputer strobe input (for various internal settings)
47	SI	DI	Serial communication microcomputer data input (for various internal settings)
48	SCK	DI	Serial communication microcomputer clock input (for various internal settings)

*1 Type column symbols

P: Power supply or GND, DI: Digital input, DO: Digital output, AI: Analog input, AO: Analog output

*2 Connect to GND through an approximately 0.1µF capacitor.

*3 Connect to GND through an approximately 390pF capacitor.

*4 Connect to GND through an approximately 0.1µF capacitor.

General Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum clock rate	$f_{ADCKMAX}$		36			MHz
A/D converter						
Resolution				10		Bit
Differential nonlinearity error		PGA gain = 0dB		±0.5		LSB
Integral nonlinearity error		PGA gain = 0dB		±1		LSB
No missing code			Guaranteed			
Programmable gain amplifier (PGA)						
Gain adjustment resolution				1023		steps
PGA gain		Settable range	–6		42	dB
		Default (Code = 0080h)		0		dB
Optical black clamp circuit						
Level adjustment resolution				15		steps
Optical black clamp level		Settable range	0		60	LSB
		Default (Code = 1000)		32		LSB

* Unless otherwise noted, the above values are for Ta = 25°C, AV_{DD} = DV_{DD} = 3.3V, clock rate (f_{ADCK} = 36MHz), and no load.

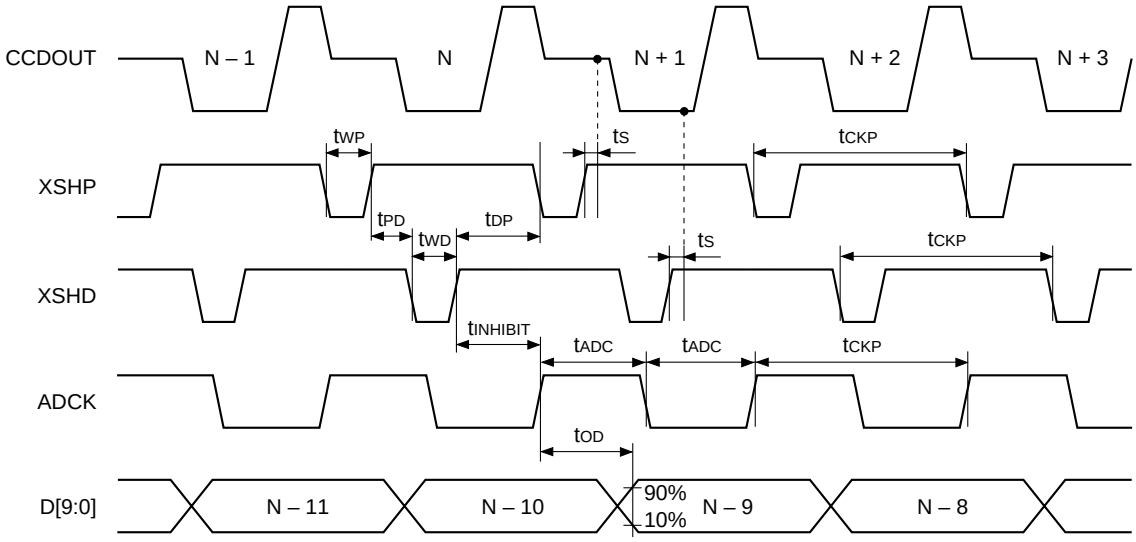
Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply						
Power consumption	PC_{MAX}	AV_{DD} = DV_{DD} = 3.3V, f_{ADCK} = 36MHz, no load		165	180	mW
	PC_{STB}	Standby mode		9	11	mW
Analog input						
Maximum input signal level		PGA gain = 0dB, full scale output	900			mV
Input capacitance	C_{INA}			15		pF
Digital input						
Input voltage	V_{IH}		2.1			V
	V_{IL}				1.1	V
Input capacitance	C_{IND}			5		pF
Digital output						
Output voltage	V_{OH}	I_{OH} = –2mA	2.7			V
	V_{OL}	I_{OL} = 2mA			0.4	V

* Unless otherwise noted, the above values are for Ta = 25°C, AV_{DD} = DV_{DD} = 3.3V, clock rate (f_{ADCK} = 36MHz), and no load.

Timing Specifications

The timing chart below shows an example of the XSHP, XSHD and ADCK phase relationships relative to the signals output from the CCD image sensor. In the CXD3301R, the A/D converter clock is generated automatically by the timing generator circuit built into the device based on XSHP and XSHD. The digital output timing is synchronized with the rising edge of ADCK.
See "Electrical Characteristics" for the XSHP, XSHD and ADCK threshold voltages.



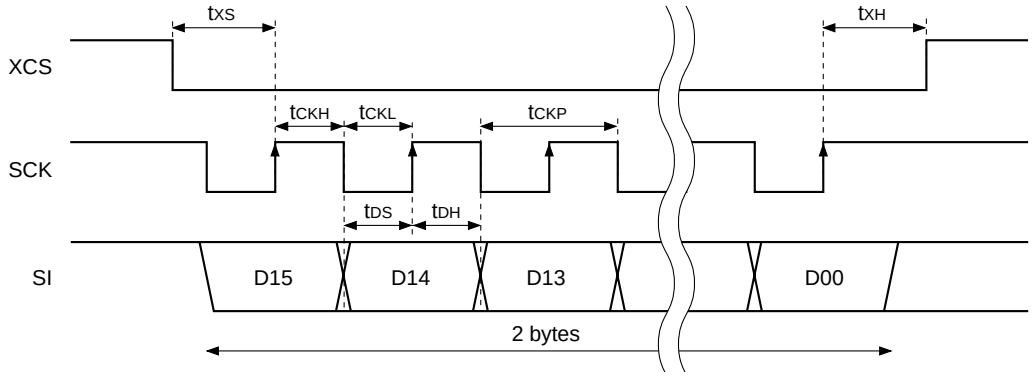
Item	Symbol	Min.	Typ.	Max.	Unit
Clock period	t_{CKP}	27.7			ns
ADCK pulse width	t_{ADC}		13.8		ns
XSHP pulse width	t_{WP}		6.9		ns
XSHD pulse width	t_{WD}		6.9		ns
Sampling delay	t_S		3		ns
Time from XSHP ↑ to XSHD ↓	t_{PD}	4			ns
Time from XSHD ↑ to XSHP ↓	t_{DP}	8			ns
Time from XSHD ↑ to ADCK ↑ (This prescribes the ADCK ↑ prohibited period.)	$t_{INHIBIT}$*1	12			ns
Output delay time	t_{OD}			18*2	ns
Data latency	DL		9 (Fixed)		clock

*1 When $t_{INHIBIT}$ is set to 12ns or less, the A/D converter may experience latch-up and it may not be possible to obtain normal images. In addition, when $t_{INHIBIT}$ is set to approximately 0ns, the data latency value changes.

*2 Load capacitance: 10pF

Serial Interface

The CXD3301R's serial interface is comprised of a 2 bytes long register, and is controlled by the two signals XCS and SCK. When data of 2 bytes or more is loaded, the last 2 bytes are valid, and the initially loaded data is lost. The data is reflected after 6 ADCK clock periods.
Avoid serial communication during the effective pixel period. Otherwise, the operation of the logic circuit block inside the CXD3301R may affect the analog circuit block, causing the picture quality to deteriorate.



Item	Symbol	Min.	Typ.	Max.	Unit
Clock period	t_{CKP}	100			ns
Clock pulse width (High)	t_{CKH}	40			ns
Clock pulse width (Low)	t_{CKL}	40			ns
Data setup time	t_{DS}	30			ns
Data hold time	t_{DH}	30			ns
Time from XCS ↓ to SCK ↑	t_{XS}	30			ns
Time from SCK ↑ to XCS ↑	t_{XH}	30			ns

The CXD3301R has the three serial communication categories of standby mode, PGA gain and optical black clamp level. The data for one category is set by one communication. When performing consecutive communication, leave a period of 5 ADCK clocks between the rise of XCS for previous communication and the fall of XCS for next communication. Table 1 shows the serial data format. Do not change bits noted as "Fixed" in the table. The CXD3301R's serial interface is MSB first, so transmit the data from the MSB.

Table 1. Serial Data Format

Bit	Category		
	Standby mode	PGA gain	Optical black clamp level
D15 (MSB)	0 (Fixed)	0 (Fixed)	0 (Fixed)
D14	0 (Fixed)	0 (Fixed)	0 (Fixed)
D13	0 (Fixed)	0 (Fixed)	1 (Fixed)
D12	0 (Fixed)	1 (Fixed)	0 (Fixed)
D11	0 (Fixed)	0 (Fixed)	0 (Fixed)
D10	0 (Fixed)	0 (Fixed)	0 (Fixed)
D09	0 (Fixed)	G9	0 (Fixed)
D08	0 (Fixed)	G8	0 (Fixed)
D07	0 (Fixed)	G7	0 (Fixed)
D06	0 (Fixed)	G6	0 (Fixed)
D05	0 (Fixed)	G5	0 (Fixed)
D04	0 (Fixed)	G4	0 (Fixed)
D03	0 (Fixed)	G3	O3
D02	0 (Fixed)	G2	O2
D01	0 (Fixed)	G1	O1
D00 (LSB)	C0	G0	O0

Table 2 shows the setting contents and default values for each category. In the CXD3301R, the serial setting values are set to the default values by performing reset. The reset pulse width (low period) is 100ns (min.).
Be sure to perform power-on reset. The setting values are undetermined at power-on, so correct operation is not possible unless power-on reset is performed.

Table 2. Setting Contents and Default Setting Values for Each Category

Category		Setting contents	Default
Standby mode	C0	C0 = 0: Normal drive C0 = 1: Standby mode	C0 = 0: Normal drive
PGA gain	G[9:0]	See "Programmable Gain Amplifier".	G[9:0] = 0080h Gain: 0dB
Optical black clamp level	O[3:0]	See "Optical Black Clamp".	O[3:0] = 1000 Clamp level: 32 LSB

Description of Functions

The CXD3301R processes (correlated double sampling, programmable gain amplifier) the signals output from a CCD image sensor and performs conversion from analog signals to digital signals. The output from the CCD image sensor is first sent to the CDS block. After that it is sent to the A/D converter block via the programmable gain amplifier (PGA) block.

Programmable Gain Amplifier (PGA)

The programmable gain amplifier (PGA) block can control the gain value by inputting a digital code via the serial interface. See Fig. 1 PGA Gain Characteristics for the relationship between the input digital code and the gain. The control range is from –6 to +42dB.

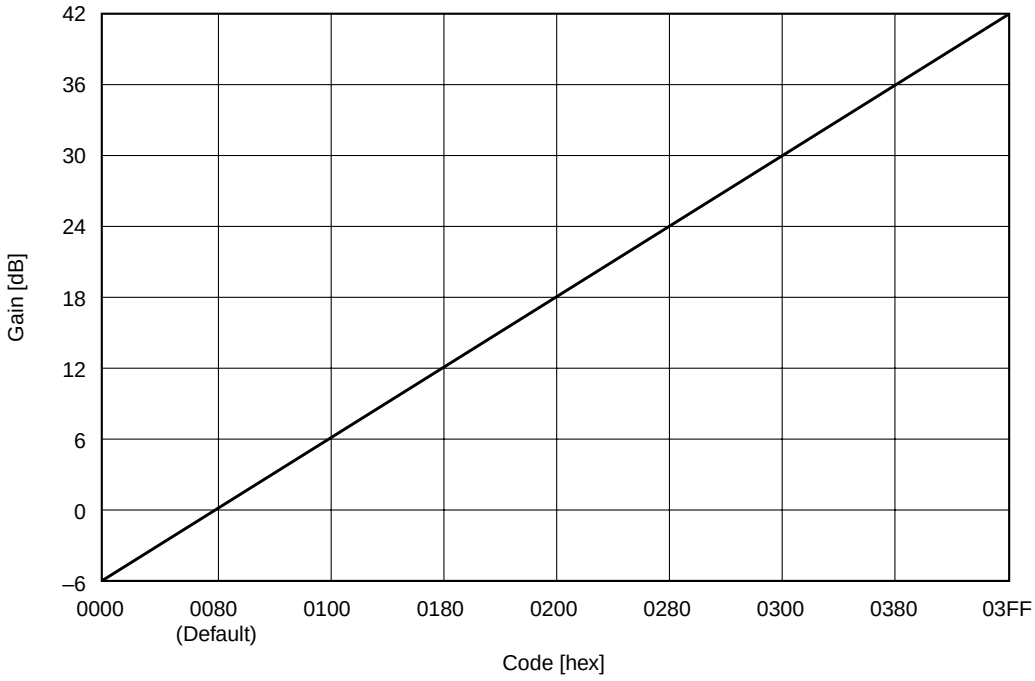


Fig. 1 PGA Gain Characteristics

Optical Black Clamp

The optical black clamp level can be set by the serial interface. (See Table 3.) See "Serial Interface" for the optical black clamp level setting method.

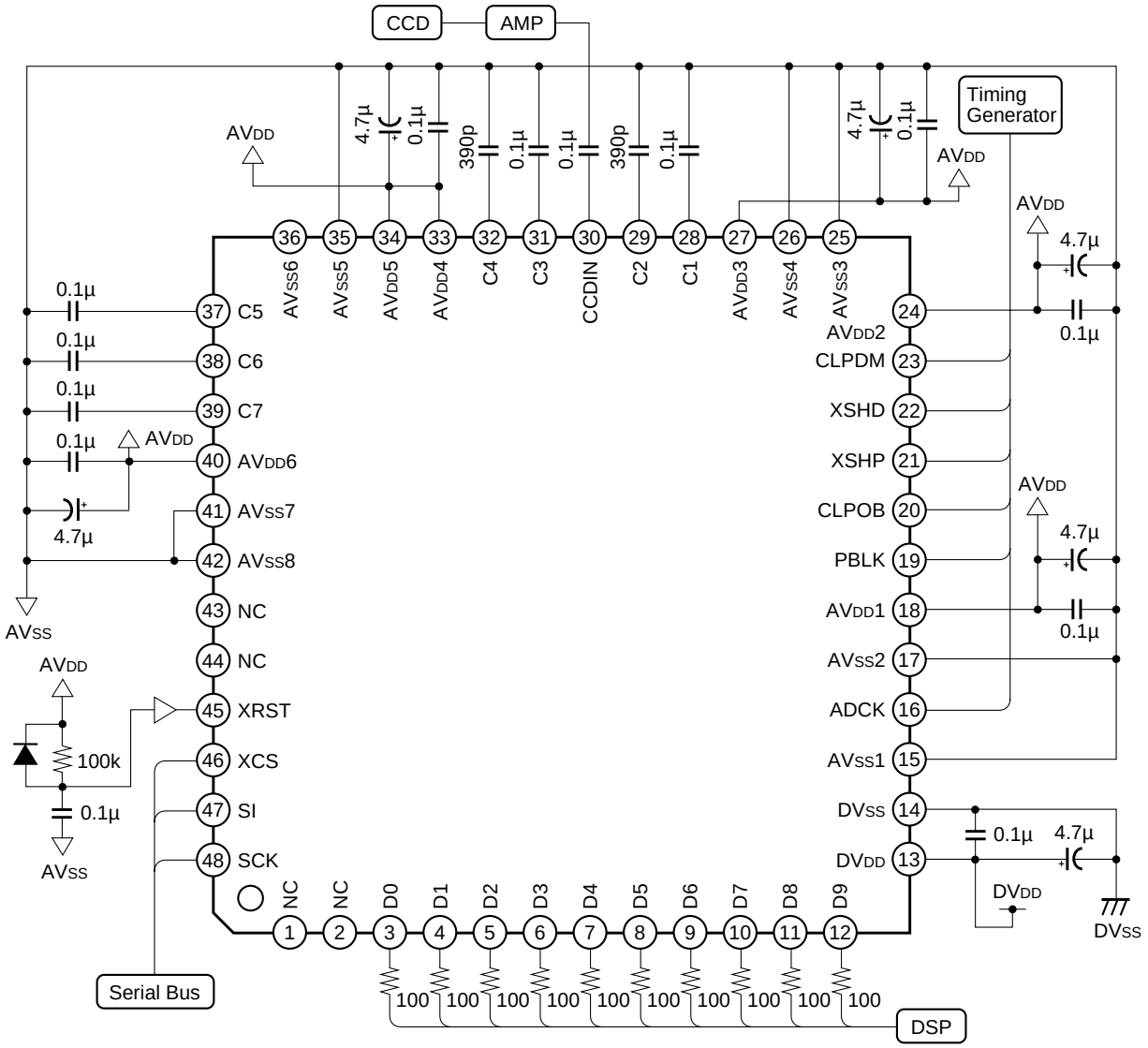
Table 3. Input Codes and Set Optical Black Clamp Level

O[3:0]					Clamp level
Decimal notation	O3	O2	O1	O0	
0	0	0	0	0	0 LSB
1	0	0	0	1	4 LSB
2	0	0	1	0	8 LSB
3	0	0	1	1	12 LSB
4	0	1	0	0	16 LSB
5	0	1	0	1	20 LSB
6	0	1	1	0	24 LSB
7	0	1	1	1	28 LSB
8 (Default)	1	0	0	0	32 LSB
9	1	0	0	1	36 LSB
10	1	0	1	0	40 LSB
11	1	0	1	1	44 LSB
12	1	1	0	0	48 LSB
13	1	1	0	1	52 LSB
14	1	1	1	0	56 LSB
15	1	1	1	1	60 LSB

Standby Mode

The CXD3301R has a standby mode, and can suppress power consumption. Activation of standby mode and recovery from standby mode is controlled via the serial interface. The serial interface and register are active even in standby mode.

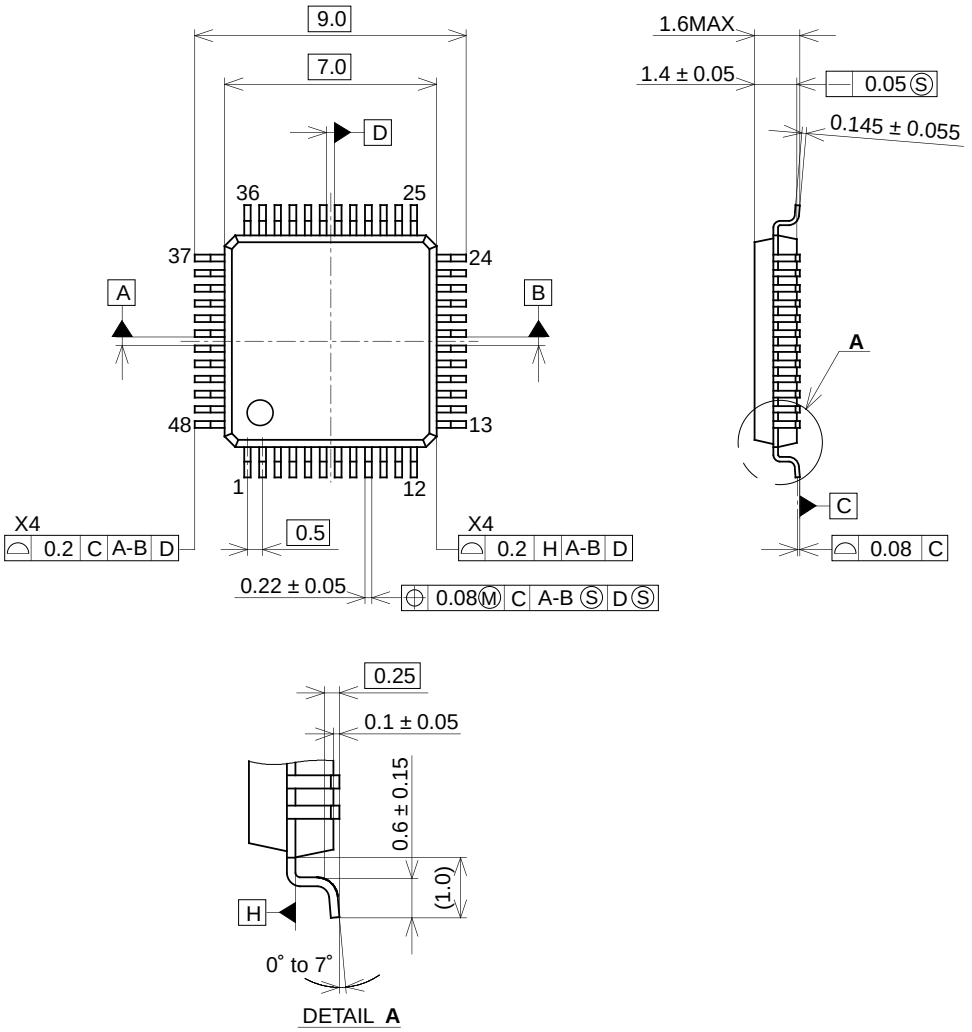
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



SONY CODE	LQFP-48P-L122
JEITA CODE	P-LQFP48-7.0x7.0-0.5
JEDEC CODE	MS-026-BBC

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.18g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm